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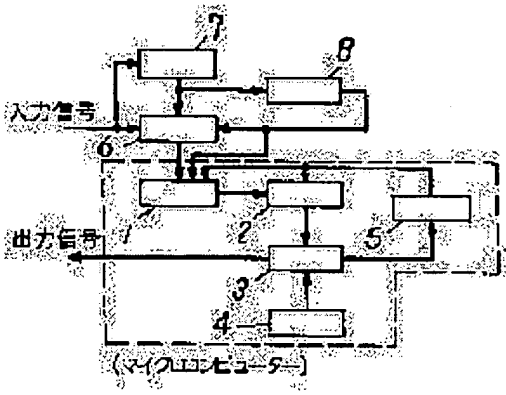
(54) SYNCHRONIZING SIGNAL DETECTOR



(57)Abstract:

PURPOSE: To accurately detect a frame synchronizing signal to send the head of information, to simplify the circuit and to reduce current consumption.

CONSTITUTION: First shift registers 1, 2 in 8-bit fetch a signal in 8-bit and the signal is compared with a signal in 8-bit being a content of a frame synchronization storage means 4 by a comparator means 3. When dissident, the 1st and 2nd shift registers 1, 2 are shifted by a control means 5 and one bit in the 1st shift register 1 is stored in the 2nd shift register 2 and the similar comparison is executed again. All frame synchronizing signals are detected through the series of operation as above.

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CLAIMS

[Claim(s)]

[Claim 1] A bit synchronization detection means to determine the sampling position of an input signal and to generate a sampling pulse, The sampling pulse from said bit synchronization detection means n bit count The counter which carries out and takes out an output signal, The buffer which carries out n bit sampling of the input signal, and saves it by the sampling pulse from said bit synchronization detection means, The 1st shift register and 2nd shift register 2 which are transmitted and saved when the output signal from said counter produces the contents of said buffer, A frame synchronization storage means by which the frame alignment signal for transmitting an informational head is memorized beforehand, The comparison means which takes out an output signal according to whether compare the contents of said 2nd shift register and said frame synchronization storage means, and the contents are in agreement, Synchronizing signal detection equipment which established the control means to which the signal from said comparison means is received and only the number of bits according to the signal shifts the contents of said 1st shift register and said 2nd shift register.

[Claim 2] Synchronizing signal detection equipment according to claim 1 which prepares the 1st shift register and 2nd shift register on the random access memory of a microcomputer, and controls a comparison means and a control means in the central processing unit of a microcomputer.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] In case this invention transmits data using a wireless electric-wave signal, it relates to the synchronizing signal detection equipment which detects the frame alignment signal for making the head of the data sent to a receiver side recognize.

[0002]

[Description of the Prior Art] The block diagram having shown the contents of the radio set in drawing 3 is shown. 9 is an antenna and 10 is a recovery means. 11 plays the role which is a filter and removes a noise. 12 is amplifier (amplifier). 13 is a comparator and

is a waveform shaper which changes an analog signal into a digital signal. A bit synchronization detection means by which 14 builds a sampling pulse, a frame synchronization detection means by which 15 doubles the timing of an informational head, and 16 are information detection means.

[0003] If an electric wave is caught with an antenna 9, the signal to which it restored through the recovery means 10 will come out. It puts on an electric wave and a bit synchronization signal is sent at first. A bit synchronization signal is for taking the synchronization for every bit which constitutes a sign, and is 1010. -- It is constituted by signal. The bit synchronization detection means 14 detects this bit synchronization signal, the sampling position of a signal is determined and a frame alignment signal is detected next according to that sampling position. Here, a 31-bit M sequence sign is made into a frame alignment signal. By detecting this frame alignment signal, an informational head can be recognized and information detection is performed one by one according to a sampling pulse.

[0004] The block diagram of drawing 4 (a) and the flow chart of drawing 4 (b) explain conventional frame alignment signal detection equipment. The number of the flow chart of drawing 4 (b) is equivalent to the number of the block diagram of drawing 4 (a) here.

[0005] 17 is 31 bit-shift register. 18 is a comparison means and compares the contents of the shift register 17 with the contents of the frame alignment signal of normal. 19 is a frame synchronization storage means to save the contents of frame synchronization beforehand. 31 bit-shift register 17 incorporates the contents of the signal received according to the sampling pulse outputted from the bit synchronization detection means of drawing 3 , and compares them with the frame synchronization storage means 19 through 31 bits and the comparison means 18 of a frame alignment signal of recognizing beforehand. When not in agreement, whenever the comparison means 18 incorporates 1 bit of input signals, it shifts and it compares the contents of the 31 bit-shift register 17. It carries out by repeating the above actuation, the time of a comparison result being in agreement is considered as establishment of frame synchronization, a shift register is reset, and then information is incorporated.

[0006]

[Problem(s) to be Solved by the Invention] However, with the above-mentioned conventional configuration, since the hardware which constitutes 31 bit-shift register must be prepared, a circuit becomes complicated. Moreover, when a shift register tended to be prepared on the memory of a microcomputer and the software of a microcomputer tended to detect a frame alignment signal, since the comparison etc. had to be processed whenever it incorporated the 1-bit signal, the technical problem that processing was asked for quickness occurred.

[0007] This invention solves the above-mentioned technical problem, and can realize it easily by software processing of a microcomputer, and it aims at offering the synchronizing signal detection equipment which attained the simplification and low-current-izing of a circuit by this.

[0008]

[Means for Solving the Problem] In order to attain the above-mentioned purpose the synchronizing signal detection equipment of this invention A bit synchronization detection means to determine the sampling position of an input signal and to generate a sampling pulse, The counter which carries out the n bit (n: integer) count of the sampling

pulse from said bit synchronization detection means, and takes out an output signal, The buffer which carries out n bit sampling of the input signal, and saves it by the sampling pulse from said bit synchronization detection means, The 1st shift register and 2nd shift register which are transmitted and saved when the output signal from said counter produces the contents of said buffer, A frame synchronization storage means by which the frame alignment signal for transmitting an informational head is memorized beforehand, The comparison means which takes out an output signal according to whether there is any paddle whose contents compares the contents of said 2nd shift register and said frame synchronization storage means, and correspond, The control means to which the signal from said comparison means is received and only the number of bits according to the signal shifts the contents of said 1st shift register and said 2nd shift register 2 is established.

[0009]

[Function] When it detects a comparatively long frame alignment signal by the above-mentioned configuration, it will store a signal in a buffer the whole n bits, and since this invention does a comparison activity with a part of frame alignment signal memorized beforehand, only the shift activity of a shift register can compare it, the contents of the buffer will be transmitted to a shift register, and it can catch [processing becomes easy and] a signal correctly.

[0010]

[Example] One example of this invention is explained below with reference to the block diagram of drawing 1 , and the flow chart of drawing 2 . The number of the flow chart of drawing 2 is equivalent to the number of the block diagram of drawing 1 here.

[0011] In drawing 1 , the 1st shift register 1 and 2nd shift register 2 are 8 bit-shift register. 3 is a comparison means to compare the contents of the signal. 4 is a frame synchronization storage means to memorize the frame alignment signal beforehand, and is 31 bit patterns. The control means by which 5 controls a shift register, and 6 are buffers which save a signal. A bit synchronization detection means by which 7 generates a sampling pulse, and 8 are counters. Here, 1-5 consist of microcomputers.

[0012] According to the sampling pulse made with the bit synchronization detection means 7, 8 bits of signals are incorporated to a buffer 6. If 8 bits is incorporated by the buffer 6 here, an output signal will arise from eight bit counters 8, and it is inputted into the 1st shift register 1 whose contents of the buffer 6 are 8 bits. If 8 bits is inputted into the 1st 8-bit shift register 1, the comparison means 3 takes out the first 8 bits of the contents of the frame synchronization storage means 4, and measures them with the contents of the 2nd shift register 2. When the result is not in agreement, the comparison means 3 outputs a signal to that effect to a control means 5. a control means 5 shifts the 2nd shift register 2 and 1st one shift register 1, and incorporates 1 bit which saw and came out from the 1st shift register 1 to the 2nd shift register 2 here. And the comparison means 3 measures the first 8 bits of the frame synchronization storage means 4, and 8 bits of the 2nd shift register 2. when not again in agreement, the comparison means 3 outputs a signal to that effect to a control means 5, and a control means 5 shifts the 2nd shift register 2 and 1st one shift register 1, and it incorporates 1 bit which saw and came out from the 1st shift register 1 to the 2nd shift register 2. And the comparison means 3 measures the first 8 bits of the frame synchronization storage means 4, and 8 bits of the 2nd shift register 2. If the same activity is repeated and the contents of the 1st shift

register 1 become empty hereafter, it will wait to input a 8-bit signal into a buffer 6 next. And when a 8-bit signal is inputted, eight bit counters 8 take out an output signal to a buffer 6 and the 1st shift register 1, and are inputted into the 1st shift register 1 whose contents of the buffer 6 are 8 bits.

[0013] When the contents of the 2nd shift register 2 and the 8-bit contents of the frame synchronization storage means are in agreement, the comparison means 3 takes out a signal to that effect to a control means 5, and a control means 5 shifts the 1st shift register 1, and incorporates the m bits the number of bits which remains in the 1st shift register 1 at the time, i.e., m times, (m: integer) to the 2nd shift register 2. And waiting and when 8 bits is inputted, eight bit counters take out an output signal for a 8-bit signal being inputted into a buffer 6, and the contents of the buffer 6 are transmitted to the 1st shift register 1. If the contents of the buffer 6 are transmitted to the 1st shift register 1, a control means 5 will carry out the time (8-m) shift of the 1st shift register 1. Furthermore, a ** (8-m) bit is incorporated to the 2nd shift register 2 by ****. The comparison means 3 compares the 8-bit contents next to the frame synchronization storage means 4 with the contents of the 2nd shift register 2 after it.

[0014] Thus, since a frame alignment signal is a 31-bit M sequence sign when the contents of the 2nd shift register 2 and the contents of the frame synchronization storage means 4 are in agreement 24 bits, the remainder becomes 31-(8*3) =7 bit. Therefore, the comparison means 3 measures the time [4th] 7 bits of the 8 bits of the contents of the 2nd shift register 2 and 7 bits of the last of the contents of the frame synchronization storage means. When a result is not in agreement, the comparison means 3 outputs a signal to that effect to a control means 5. With the output signal from the comparison means 3, a control means 5 cancels all the contents of the 1st shift register 1 and the 2nd shift register 2 in the 24-bit frame alignment signal list which is already in agreement, and redoes comparison / detection activity from the beginning here. When a result is in agreement, it means detecting all 31 bits of frame alignment signals, and the comparison means 3 takes out an output signal to that effect.

[0015] Here, if 1 bit of arbitration is beforehand added to the 31 bits of the contents of the frame synchronization storage means 4, it is made 32 bits and the same measures also as a transmitter side are taken, the comparison means 3 can detect all 31 bits of frame alignment signals by doing the comparison activity in every 8 bits 4 times simply, and can simplify software processing with a microcomputer more.

[0016] In addition, the number of bits of a frame alignment signal which is in agreement if 1 bit shifts, since it is a 31-bit M sequence sign decreases extremely. Therefore, it can also be made the configuration of the signal detection to which the error of a frame alignment signal is permitted to 2 error extent.

[0017] According to the configuration of this example, since it is altogether realizable with a microcomputer if an easy 8-bit buffer and an easy counter are removed, the complexity of a circuit is cancelable. In order to do a comparison activity every 8 bits on memory furthermore, when doing a comparison activity for every bit, the place which needs 32 / 8= 4 shift registers If the 1st 8-bit shift register 1 becomes empty, a buffer can be compensated with 8 bit data being incorporated with two shift registers waiting and by transmitting data to the 1st 8-bit shift register 1, as soon as it is incorporated, and memory space can be reduced this time. Moreover, processing is quickly completed until it incorporates a 8-bit signal to a buffer and then incorporates 8 bits, and actuation of a

microcomputer can be suspended temporarily and it is effective in the ability to aim at reduction of the consumed electric current.

[0018]

[Effect of the Invention] As explained above, when the synchronizing signal detection equipment of this invention detects a comparatively long frame alignment signal, a signal will be stored in a buffer the whole n bits, since a comparison activity is done with a part of frame alignment signal memorized beforehand, only the shift activity of a shift register can compare, the contents of the buffer will be transmitted to a shift register, and a signal can be caught [processing becomes easy and] correctly. Furthermore, since it is realizable by the software of a microcomputer, and easy hardware, equipment itself can attain simplification and it can lower a manufacturing cost. Moreover, by attaining low current-ization, a battery life etc. can be developed and it is effective in increasing commodity value.